

## **Mobile Double Data Rate (DDR) SDRAM**

### MT46H16M16LF – 4 Meg x 16 x 4 Banks MT46H8M32LF – 2 Meg x 32 x 4 Banks

For a complete data sheet, please refer to www.micron.com/mobileds.

#### **Features**

- $VDD = +1.8V \pm 0.1V$ ,  $VDDQ = +1.8V \pm 0.1V$
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- · Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; centeraligned with data for WRITEs
- · Four internal banks for concurrent operation
- Data masks (DM) for masking write data-one mask per byte
- Programmable burst lengths: 2, 4, 8, 16 or full page
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS compatible inputs
- · On-chip temperature sensor to control refresh rate
- Partial array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive (DS)
- Clock stop capability

# Options Marking • VDD/VDDQ

	• 1.8V/1.8V	
•	Configuration	

16 Meg x 16 (4 Meg x 16 x 4 banks)
 8 Meg x 32 (2 Meg x 32 x 4 banks)
 8M32

Plastic Package

• 60-Ball VFBGA<sup>1</sup> TBD

• 90-Ball VFBGA <sup>2</sup>

• Timing – Cycle Time

• 6ns @ CL = 3 -6 • 7.5ns @ CL = 3 -75

• 10ns @ CL = 3

Operating Temperature Range

• Commercial (0° to +70°C) None

• Industrial (-40°C to +85°C)

Notes:1. Only available for x16 configuration.
2. Only available for x32 configuration.

### Figure 1: 60-Ball VFBGA Assignment

	1	2	3	4	5	6	7	8	9
Α	Vss	DQ15	VssQ	$\bigcirc$	$\bigcirc$	$\bigcirc$	VDDQ	DQ0	VDD
В	VDDQ	DQ13	DQ14	$\bigcirc$	$\bigcirc$	$\bigcirc$	DQ1	DQ2	VssQ
С	VssQ	DQ11	DQ12	$\bigcirc$	$\bigcirc$	$\bigcirc$	DQ3	DQ4	VDDQ
D	VDDQ	DQ9	DQ10	$\bigcirc$	$\bigcirc$	$\bigcirc$	DQ5	DQ6	VssQ
E	VssQ	UDQS	DQ8	$\bigcirc$	$\bigcirc$	$\bigcirc$	DQ7	LDQS	VDDQ
F	Vss	UDM	O NC	$\bigcirc$	$\bigcirc$	$\bigcirc$	A13, NC	LDM	VDD
G	CKE	○ CK	CK#	$\bigcirc$	$\bigcirc$	$\bigcirc$	WE#	CAS#	RAS#
Н	A9	A11	A12	$\bigcirc$	$\bigcirc$	$\bigcirc$	CS#	O BA0	O BA1
J	A6	A7	A8	$\bigcirc$	$\bigcirc$	$\bigcirc$	A10/AP	A0	A1
K	Vss	A4	A5	$\bigcirc$	$\bigcirc$	$\bigcirc$	A <sub>2</sub>	A3	VDD

### **Table 1: Configuration Addressing**

Architecture	16 Meg x 16	8 Meg x 32
Configuration	4 Meg x 16 x 4	2 Meg x 32 x 4
Refresh Count	8K	4K
Row Addressing	8K (A0-A12)	4K (A0-A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	1K (A0-A9)	1K (A0-A9)

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Advance: This data sheet contains initial descriptions of products still under development.



### 256Mb: 16 Meg x 16, 8 Meg x 32 Mobile DDR SDRAM

R	evision History	
•	Original Document, Preview0	3/05